

In re Patent Application of:
SANCHES ET AL.
Serial No. 09/915,761
Filing Date: JULY 26, 2001

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59.

The title has been changed to be more specific as requested by the Examiner. The arguments supporting patentability of the claims are presented in detail below.

I. The Independent Claims Are Patentable

Independent Claims 20, 31, 41 and 50 have been rejected over the Faraboschi et al. patent in view of the Bratt et al. patent and in further view of the Hennessy et al. article titled "Computer Architecture A Quantitative Approach."

Independent Claim 31 is directed to a processor for executing variable-sized instructions, with each instruction comprising up to N codes with N being a positive integer greater than 1. The processor comprises a memory comprising I individually addressable, parallel-connected memory banks with I being a positive integer at least equal to N. The memory comprises a program recorded in an interlaced fashion as a function of one code per memory bank and per address applied to the memory banks.

A reading circuit reads the memory by reading a code in each of the I memory banks during a cycle for reading an instruction, with each instruction comprising a sequence of codes to be read and when a number of the sequence of codes of the instruction being read is less than I, then codes

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belonging to a following instruction are read.

The reading circuit comprises an address circuit and a filtering circuit. The address circuit applies to the memory banks individual addresses generated from a collective value of a program counter that is incremented, before a beginning of the cycle for reading the instruction, by a value equal to a number of codes belonging to a previous instruction, and applies to each of the memory banks an individual read address that is based upon a result of a division by I of the collective value of the program counter. The filtering circuit filters codes that do not belong to the instruction to be read, while using parallelism bits accompanying the codes.

Independent device Claim 20 is similar to independent device Claim 31 except the reading circuit, address circuit and filtering circuit have been replaced with reading means, address means and filtering means. Independent method Claim 41 is similar to independent device Claim 31. Independent method Claim 50 is similar to independent method Claim 41 except the step of providing a program memory is in the preamble of the claim instead of the body of the claim.

Referring now to the Faraboschi et al. patent, the Examiner cited Faraboschi et al. as disclosing a program memory comprising I individually addressable, parallel-connected memory banks, and a reading circuit for reading the program memory. The Examiner also cited Faraboschi et al. as disclosing that the program memory comprises a program recorded in an interlaced fashion, and that the reading circuit reads a code in each of the I memory banks during a cycle for reading an instruction. When a number of codes of

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the instruction to be read is less than I, Faraboschi et al. discloses that codes belonging to a following instruction are read.

The Examiner further cited Faraboschi et al. as disclosing an address circuit for applying to the memory banks individual addresses generated from a collective value of a program counter that is incremented (column 4, lines 29-30) before a beginning of the cycle for reading the instruction, by a value equal to a number of codes comprising a previous instruction (column 2, lines 13-30). The Examiner states that it is inherent that a read address be calculated before the cycle in which the read is performed. A filter circuit filters codes that do not belong to the instruction to be read, using parallelism bits accompanying the codes (column 4, line 57 through column 5, line 5).

As correctly noted by the Examiner, Faraboschi et al. does not teach that the program recorded in the program memory is done so in an interlaced fashion as a function of one code per memory bank. The Examiner cited the Bratt et al. patent as disclosing this feature (col. 1, lines 29-64) of the present invention. The Examiner has taken the position that it would have been obvious to modify the processor in Faraboschi et al. to store consecutive instruction codes in consecutive memory banks in an interlaced fashion as a function of one code per memory bank, as disclosed in Bratt et al.

In addition, as correctly noted by the Examiner, Faraboschi et al. in view of Bratt et al. does not teach applying to each of the memory banks an individual read address that is based upon a result of a division by I of the

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collective value of the program counter. However, the Examiner has taken the position that Bratt et al. discloses in column 1, lines 31-35 that some address bits are used to determine which bank and address to address. The Examiner also correctly notes that Bratt et al. does not explicitly teach how the address bits are used to determine this operation. On page 432 of the Hennessy et al. article, interlaced memory banks are used to determine which bank to access by performing a modulo operation on the address and the number of banks. The Examiner takes the position that it would have been obvious at the time of the invention to incorporate the interleaved memory scheme of Hennessy et al. in the device of Bratt et al. to optimize sequential memory accesses.

The Applicants respectfully submit that even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. First, none of the prior art references disclose a program counter being incremented, before a beginning of a cycle for reading an instruction, by a value equal to a number of codes belonging to a previous instruction.

Faraboschi et al. discloses in FIG. 3 an address circuit 202 for applying to the memory banks 110 individual addresses generated from a collective value of a program counter 200 that is incremented before a beginning of a cycle for reading an instruction. This increment is based upon a previous instruction address for providing a successive instruction address. Reference is directed to column 4, lines 25-30 of Faraboschi et al., which provides:

"A program counter 200 provides successive

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instruction addresses of a program being executed to instruction cache 100 through an address buffer 202. Instruction addresses are also provided to a cache refill state machine 204, an adder 206 which increments program counter 200, and to a comparator 208." (Emphasis added.)

The adder 206 thus increments the program counter based upon the previous instruction address. However, the Examiner references column 2, lines 13-30 in Faraboschi et al. as disclosing that the program counter is incremented by a value equal to a number of codes comprising a previous instruction. The Applicants again respectfully disagree. Reference is directed to column 2, lines 13-30 of Faraboschi et al., which provides:

"Due to the variable length of the compressed instruction format in memory, it is necessary to record the offset to the next instruction address somewhere in the instruction itself. The offset must also be stored in the instruction cache to be able to execute correct program counter sequencing and to maintain coherency between the program counter and the main memory code image. . . . The major disadvantage of using the technique shown in FIG. 2 and described above is that consecutive instructions do not correspond to consecutive instruction cache locations, as they are separated by an address difference that depends on the variable length of the instruction." (Emphasis added.)

Faraboschi et al. thus fails to disclose that the program counter is incremented by a value equal to a number of

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codes belonging to a previous instruction, as recited in independent Claim 31.

As correctly noted above by the Examiner, Faraboschi et al. in view of Bratt et al. does not teach applying to each of the memory banks an individual read address that is based upon a result of a division by I of the collective value of the program counter. The Examiner cited the Hennessy et al. article as disclosing this feature of the claimed invention. As illustrated in FIG. 5.32 in Hennessy et al., a four-way interleaved memory is shown. This example assumes word addressing: with byte addressing and four bytes per word. Each of these addresses would be multiplied by four. Hennessy et al. also fails to disclose that a program counter is incremented by a value equal to a number of codes belonging to a previous instruction.


Accordingly, it is submitted that independent Claim 31 is patentable over the Faraboschi et al. patent in view of the Bratt et al. patent. Independent Claims 20, 41 and 50 are similar to independent Claim 31. In view of the patentability of independent Claims 20, 31, 41 and 50, it is submitted that the dependent claims which recite yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

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CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,


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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 22 day of February, 2005.